WHAT IS CLAIMED IS:

1. A single-chip microcomputer comprising:

a first bus having a central processing unit and a cache memory connected therewith;

a second bus having a dynamic memory access control circuit and an external bus interface connected therewith;

a break controller connected with said first bus and said second bus for transmitting an address signal of said first bus selectively to said second bus;

a third bus having connected therewith a peripheral module and given a lower-speed bus cycle than those of said first and second buses; and

a bus state controller coupled between said second bus and said third bus for effecting a signal transfer and a synchronization between said second bus and said third bus.

2. A single-chip microcomputer according to Claim 1,

further comprising:

a fixed point multiply and accumulate arithmetic unit connected with said first bus; and

a fixed point type divider unit connected with

said second bus.

3. A single-chip microcomputer according to Claim 1,

wherein said peripheral module includes at least one of a free running timer FRT, a serial communication interface SCI and a watch-dog timer.

4. A single-chip microcomputer according to Claim 1,

wherein said break controller has a function to monitor the rewrite of the data of the cache memory by said dynamic memory access control unit.

5. A single-chip microcomputer according to Claim 1,

wherein said individual circuit blocks are constructed of full static type CMOS circuits,

further comprising an operation mode controller including a register for controlling the feed/interrupt of a clock pulse to each of said circuit blocks.

6. A single-chip microcomputer according to Claim 1,

wherein said external bus interface includes: a

burst read mode and a single write mode of a synchronous dynamic type RAM; and an interface for accessing a dynamic type RAM and a pseudo-static type RAM directly.

7. A single-chip microcomputer according to Claim 6,

wherein said external bus interface has a function to produce a clock pulse, which has its phase advanced from the clock pulse of said central processing unit, and feed the same to the clock terminal of said synchronous dynamic type RAM.

8. A single-chip microcomputer according to Claim 6,

wherein the data size to be read out of the burst mode of said synchronous dynamic type RAM, the data size of the unit block of said cache memory, and the data size of the unit data transfer by said dynamic memory access controller have a matching among one another.

9. A single-chip microcomputer according to Claim 6,

wherein said external bus interface includes a memory control signal generator started, when said central processing unit accesses a predetermined address space, to set a row address strobe signal, a column address strobe signal and a write enable signal all together to the low level thereby to output a mode setting signal for said synchronous dynamic type RAM by using said address signal partially.

10. A single-chip microcomputer according to Claim 1,

wherein said cache memory includes: a tag memory having a plurality of memory arrays; and a data memory having a plurality of memory arrays disposed to correspond to the plurality of memory arrays of said tag memory, respectively, and

wherein each of said tag memory and said data memory includes:

a plurality of CMOS static memory cells; and

a sense amplifier having a CMOS latch circuit for amplifying the signals read out of said memory cells, and a power switch MOSFET composed of a P-channel type MOSFET and an N-channel type MOSFET for feeding an operation current to said CMOS latch circuit.

11. A single-chip microcomputer according to Claim 10,

wherein only that of the plurality of memory arrays of said data memory which corresponds to a hit signal coming from said tag memory is activated.

12. A single-chip microcomputer according to Claim 10,

wherein the plurality of memory arrays of said data memory are enabled by said cache controller to invalidate the transmission of the hit signal from said tag memory for all or a portion of said memory arrays thereby to be accessed by said central processing unit.

13. A single-chip microcomputer comprising:

a central processing unit; and

a cache memory including: a memory element of a CMOS static type memory cell; a CMOS latch circuit acting as a sense amplifier for amplifying a signal read out of said memory element; and a power switch MOSFET composed of a P-channel type MOSFET and an N-channel type MOSFET for feeding an operation current to said CMOS latch circuit.

14. A single-chip microcomputer according to Claim 13,

wherein the data memory of a plurality of memory arrays of said cache memory includes a tag memory of a plurality of memory arrays, and

wherein only that memory array of said data memory which correspond to a hit signal coming from one memory array of said tag memory is activated.

15. A single-chip microcomputer comprising an external bus interface having a function to switch and use a first terminal for a bus request signal and a second terminal for a bus acknowledge signal, when set to a slave mode in accordance with a bus use priority control signal, and to switch and use said first terminal for a bus grand signal and said second terminal for a bus release signal when set to a master mode.

16. A single-chip microcomputer according to Claim 2,

wherein said central processing unit executes a clipping processing, which has been subjected to a perspective transformation processing, of a three-dimensional image processing, and a coordinate

transformation processing for transforming a coordinate point intrinsic to a predetermined object into a coordinate having a predetermined view point as an origin point, in association with said multiply and accumulate arithmetic unit, and

wherein said divider unit executes the perspective transformation processing of the coordinate which has been subjected to the coordinate transformation processing, simultaneously in parallel with said central processing unit and said multiply and accumulate arithmetic unit.